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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,609	09/08/2003	Patrick James McGuinness	SC12009TS	1773

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,609	MCGUINNESS ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/09/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,28 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 september 2003 and 09 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/657,609 filed on 09/08/2003 and Applicant Argument filed on 12/09/2005, the remained claims 1-24 and 28-29 are pending.

2. Claims 15, 23, and 28 have been amended.

3. Claims 25-27 have been cancelled.

4. The specification is amended. Applicant's new title is approved.

5. Applicant's arguments with respect to claims 1-8, 14-22, 23-24, and 28-29 have been considered but are moot in view of the new ground(s) of rejection.

6. The indicated allowability of claims 4-8, 19-22, and 27-29 is withdrawn in view of the newly discovered reference(s) to Gupta (US 6,163,877) and Aoki (US 5,675,501). Rejections based on the newly cited reference(s) follow.

Priority

7. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Russian Federation on 09/20/2002. It is noted, however, that applicant has not filed a certified copy of the PCT/RU02/00430 application as required by 35 U.S.C. 1 19(b).

Specification

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) The Names Of The Parties To A Joint Research Agreement: See 37 CFR 1.71(g).

(e) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(g) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems

previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(h) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(i) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(j) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(k) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(l) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed

in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

8. The disclosure is objected to because of the following informalities: Examiner request that Applicant must provide the Summary of the invention in according with 37 CFR 1.73.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-3, 14-18, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Gupta (US 6,163,877).

11. **With respect to claims 1 and 16**, Gupta discloses a method for generating an integrated circuit layout (col. 3, ll. 13-15), comprising the steps of:

receiving an integrated circuit netlist describing a plurality of transistors and a plurality of conductors for interconnecting the plurality of transistors (col. 2, ll. 27-35), each of the plurality of transistors having a width in a layout corresponding to the integrated circuit netlist (col. 2, ll. 27-35, col. 6, ll. 60-67, col. 7, ll. 1-13 and figures 5-7 see their descriptions);

determining that more than one of the plurality of transistors are the widest transistors and that the more than one widest transistors all have the same width

(figures 7A-7B, Transistors N1, N2, N3, are widest (highest) transistors and have a same width (high));

folding only one of the widest transistors to produce a folded transistor that is electrically equivalent to the widest transistor (figures 7A-7B and col. 5, ll. 48-67 and col. 6, ll. 1-8, --each transistor N1, N2, and N3 fold into three fold. Moreover, refer to figure 5, fold only one of the widest transistor [F] --), the folded transistor having at least two fingers, each finger having a smaller width than the width of the widest transistors (col. 1, ll. 63-67 and col. 2, ll. 11-8); and

creating a fold solution for the layout with the one folded transistor (col. 7, ll. 33-40, figures 5-7, as exemplary of figure 5, element [508] is fold solution of element [502]).

12. **With respect to claim 14**, Gupta disclose a method for generating an integrated circuit layout (col. 3, ll. 13-15) comprising the steps of:

receiving a base logical cell structure describing a plurality of transistors and a plurality of conductors for interconnecting the plurality of transistors, each of the transistors having a width in a layout corresponding to the base logical cell structure (col. 2, ll. 27-35, col. 6, ll. 60-67, col. 7, ll. 1-13 and figures 5-7 see their descriptions);

iteratively folding only one transistor at a time (individual fold) of the plurality of transistors that have a width greater than a predetermined width to produce two transistors (figure 9, step 906, col. 7, ll. 33-40) , each of the two transistors having a width shorter than the width of a corresponding unfolded transistor (col. 1, ll. 63-67 and col. 2, ll. 11-8); and

after each iteration, creating a fold solution after each iteration and adding the fold solution to a fold solution list (figure 9, steps 910 and 912, storing fold list, col. 8, l. 8-46 -- a transistor chains is of one transistor first, the transistor chains of increasingly larger number of transistor are formed--).

13. **With respect to claims 2 and 17**, Gupta discloses the method of claim 1, wherein the steps of folding and creating are repeated (recursive branch and bound) for each of the plurality of transistors until all of the plurality of transistors have been folded at least once (figure 9, steps 914-918, col. 9, ll. 30-50 and col. 10, ll. 1-16).

14. **With respect to claims 3 and 18**, Gupta discloses the method of claim 2, wherein the plurality of transistors includes a plurality of N-channel transistors and a plurality of P-channel transistors and the steps of folding and creating are repeated for each transistor of the plurality of N-channel transistors to create an independent (unpaired transistor) N-channel fold solution list and the steps of folding and creating are repeated for each transistor of the plurality of P-channel transistors to create an independent P-channel fold solution list (unpaired transistor) (figure 9, step 908, col. 7, ll. 40-57--unpaired transistor is may exist – step 916, col. 10, ll. 1-17).

15. **With respect to claim 15,** Gupta disclose the method of claim 14, wherein the base logical cell structure is a portion of an integrated circuit netlist for defining an integrated circuit (figure 10, col. 6, ll. 60-67, col. 7, ll. 1-32).

16. **With respect to claim 23,** Gupta discloses a method (col. 3, ll. 13-15) for generating an integrated circuit layout comprising the steps of:

receiving an integrated circuit netlist describing a plurality of P-channel transistors, a plurality of N-channel transistors, and a plurality of conductors for interconnecting the plurality of N-channel transistors and the plurality of P-channel transistors, each of the transistors having a width in a layout corresponding to the integrated circuit netlist (Gupta, col. 2, ll. 27-35, figure 4, col. 4, ll. 23-43);

folding the widest transistors of the plurality of N-channel transistors and the plurality of P-channel transistors to produce a list of folded N-channel transistors and a list of folded P-channel transistors, each folded transistor having at least two fingers, each finger having a smaller width than the width of its corresponding unfolded transistor, and each folded transistor being electrically equivalent to its corresponding unfolded transistor (figure 8, col. 6, ll. 38-59, and figure 9, step 908);

receiving a dependency map for listing dependent pairs of N-channel and P-channel transistors (pair P/N transistor) from the integrated circuit netlist (Gupta, figure 10-12, see their descriptions);

folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount (exceeding a certain height) to produce an N-channel dependent fold list and a P-channel dependent fold list (Gupta, figure 9, step 908, col. 7, ll. 40-67 and col. 8, ll. 1-65); and

merging the list of folded N-channel transistors, the list of folded P-channel transistors (P/N pairs), the N-channel dependent fold list and the P-channel dependent fold list (list of pair can share their diffusions) to produce an initial fold solution list

(Gupta, figure 12A, list 1202, col. 8, ll. 8-46, -- a transistor chains is of one transistor first, the transistor chains of increasingly larger number of transistor are formed--).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 4-13, 19-24, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (US 6,163,877) in view of Aoki (US 5,675,501).

19. **With respect to claims 4, 9, 19, and 24,** Gupta teaches a method for generating an integrated circuit layout comprising the steps of:

(claim 9) receiving an integrated circuit netlist describing a plurality of P-channel transistors, a plurality of N-channel transistors, and a plurality of conductors for interconnecting the plurality of N-channel transistors and the plurality of P-channel transistors, each of the transistors having a width in a layout corresponding to the integrated circuit netlist (Gupta, col. 2, ll. 27-35, figure 4, col. 4, ll. 23-43);

(claim 9) folding the widest transistors of the plurality of N-channel transistors and the plurality of P-channel transistors to produce a list of folded N-channel transistors and a list of folded P-channel transistors, each folded transistor having at least two fingers, each finger having a smaller width than the width of its corresponding unfolded transistor, and each folded transistor being electrically equivalent to its corresponding unfolded transistor (figure 8, col. 6, ll. 38-59, and figure 9, step 908);

(claims 4, 9, and 19) receiving a dependency map for listing dependent pairs of N-channel and P- channel transistors (pair P/N transistor) from the integrated circuit netlist (Gupta, figure 10-12, see their descriptions);

(claims 4, 9, and 19) folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount (exceeding a certain height) to produce an N-channel dependent fold list and a P-channel dependent fold list (Gupta, figure 9, step 908, col. 7, ll. 40-67 and col. 8, ll. 1-65); and

(claims 4, 9, and 19) merging the list of folded N-channel transistors, the list of folded P-channel transistors (P/N pairs), the N-channel dependent fold list and the P-channel dependent fold list (list of pair can share their diffusions) to produce an initial fold solution list (Gupta, figure 12A, list 1202, col. 8, ll. 8-46, -- a transistor chains is of one transistor first, the transistor chains of increasingly larger number of transistor are formed--).

Gupta teaches steps of transistor folding under maximum height specified by the user (Gupta, col. 7, ll. 33-40).

Gupta does not teach steps of (claims 4, 9, 19, and 24) generating a height lower bound by summing up the widths of the dependent pairs.

Aoki teaches the step calculating (generating) a predetermined height by summing up the widths of dependent pairs (Aoki, col. 6, ll. 15-39).

Therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to combine Gupta and Aoki for generating a predetermined height value of using determined size transistor which has the width (height) exceed the

predetermined height value, and then performed the transistor arrangement or folding, (Gupta, col. 4, ll. 12-15 and Aoki, col. 5, ll. 55-60) to eliminate dead space occurring between the transistor layout within an integrated circuit (Aoki, col. 4, ll. 10-15).

20. With respect to claims 5, 10, 20, and 28, Gupta and Aoki teach the method of the claims they dependent from, and further comprising the step of selecting a fold solution from the initial fold solution list (initial fold solution list may obtained unpaired and pairs transistors) (Gupta, figure 9, step 910, col. 8, ll. 846, -- this stage just selects only pairs transistor --).

21. With respect to claims 6, 11, 21, and 29, Gupta and Aoki teach the method of the claims they dependent from, and further comprising the step of create modified fold solution from the selected fold solution based on predetermined cell layout information (Gupta, col. 8, ll. 55-67 and col. 10, ll. 1-6).

22. **With respect to claims 7, 12, and 22,** Gupta and Aoki teach the method of the claims they dependent from, and further comprising the steps of:

placing transistors from the modified fold solution list (introducing unpaired into fold solution list) in the integrated circuit layout (Gupta, figure 9, refined step 918 to 910, col. 10, ll-6-12);

defining a routing channel between the plurality of P-channel transistors and the plurality of N-channel transistors (Gupta, col. 9, ll. 50-67);

calculating a predetermined metric for the modified fold solution (Gupta, figure 9, step 912, col. 1-6, -- generating chain cover --); and

generating the integrated circuit layout (Gupta, figure 9, step 922 [cell layout]).

23. **With respect to claims 8 and 13,** Gupta and Aoki teach the method of the claims they dependent from, and wherein the method is implemented as software on a data processing system (Gupta, col. 10, ll. 37-50).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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